VOLTAGE-VARIABLE DELAY LINE
TR < 1ns
(SERIES 3010)

FEATURES

• Varactor Technology
• Fast rise time for high frequency applications
• Delay continuously adjustable from 2.4ns to 3.4ns
• Very narrow device (SIP package)
• Stackable for PC board economy
• Epoxy encapsulated
• Meets or exceeds MIL-D-23859C

FUNCTIONAL DESCRIPTION

The 3010-series devices are continuously variable, single-input, single-output, passive delay lines. The signal input (IN) is reproduced at the output (OUT), shifted by a time (TD) which is adjusted via an applied control voltage (VC). This control voltage is positive for the 3010-P and negative for the 3010-N. The characteristic impedance of the line is nominally 50 ohms. The rise time (TR) of the lines is no more than 1ns, resulting in a 3dB bandwidth of at least 300MHz. The delay resolution is limited only by that of the control voltage.

SERIES SPECIFICATIONS

• Varactor voltage range (3010-P): 1.3V (max TD) to 11.3V (min TD)
• Varactor voltage range (3010-N): -1.3V (max TD) to -11.3V (min TD)
• Range of delay variation: 1.0ns minimum
• Minimum delay: 2.4ns ± 0.25ns
• Impedance: 45Ω - 68Ω
• Output rise time: 1.0ns max
• Bandwidth: 300MHz min
• Overshoot/preshoot: ± 20% max
• Operating temperature: -10°C to +80°C
• Temperature coefficient: 1000 PPM/°C max

PIN DESCRIPTIONS

IN Signal Input
OUT Signal Output
VC Control Voltage
G Ground

Series 3010

Package Dimensions

Typical Delay/Impedance Variation
TYPICAL APPLICATIONS

**Signal source impedance**

- Rin: Input termination resistor
- Ro: Output termination resistor

- Set Ro to the median impedance value within the delay adjustment range (50Ω - 60Ω)
- Set Rin = Rout - r

*Reverse polarity for 3010-N.

**Analog Interface**

**ECL with –2V Termination**

- 2.6Ro
- Vcc = 0V
- Vee = -5.2V

**ECL without –2V Termination**

- 2.6Ro
- Vcc = 0V
- Vee = -5.2V

Note: The varicap voltage is referenced to the DC level of the input signal. In the case of ECL applications, a voltage of 0V to 10V (2.6V to 12.6V for the 3010-N) should be applied at pin 6, because the signal line has –1.3V DC level. This assumes the ECL signal has approximately 50% duty cycle.
PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Input Pulse:
High = 1.8V typical
Low = 0.8V typical
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured at 10% and 90% levels)
Pulse Width: PW_in = 500ns
Period: PER in = 1000ns

OUTPUT:
Rload: 50Ω
Cload: <10pf
Threshold: 50% (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

Timing Diagram For Testing

Test Setup