MONOLITHIC 5-TAP FIXED DELAY LINE
(SERIES 3D7215 – LOW NOISE)

FEATURES

- All-silicon, low-power 5V CMOS technology
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- Delay range: 1ns through 250ns
- Delay tolerance: 2% or 1ns
- Temperature stability: ±1% typical (0C-70C)
- Vdd stability: ±0.5% typical (3.0V-3.6V)
- Static Idd: 1.5ma typical
- Minimum input pulse width: 20% of total delay

PACKAGES

- IN
- O2
- O4
- GND
- VDD
- DIP (300 Mil)
- SOIC (150 Mil)

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7215 5-Tap Delay Line product family consists of fixed-delay 5V CMOS integrated circuits. Each package contains a single delay line, tapped and buffered at 5 points spaced uniformly in time. Tap-to-tap (incremental) delay values can range from 1ns through 50ns. The input is reproduced at the outputs without inversion, shifted in time as per the user-specified dash number. The 3D7215 is 5V CMOS-compatible and features both rising- and falling-edge accuracy.

The all-CMOS 3D7215 integrated circuit has been designed as a reliable, economic alternative to hybrid fixed delay lines. It is offered in a standard 8-pin auto-insertable DIP and a space saving surface mount 8-pin SOIC.

PIN DESCRIPTIONS

IN Delay Line Input
O1 Tap 1 Output (20%)
O2 Tap 2 Output (40%)
O3 Tap 3 Output (60%)
O4 Tap 4 Output (80%)
O5 Tap 5 Output (100%)
VDD +5 Volts
GND Ground
N/C No Connection

TABLE 1: PART NUMBER SPECIFICATIONS

<table>
<thead>
<tr>
<th>DASH #</th>
<th>TOTAL DELAY (ns)</th>
<th>TAP-TAP DELAY (ns)</th>
<th>RECOMMENDED MAX FREQ</th>
<th>RECOMMENDED Min P.W.</th>
<th>ABSOLUTE Max Freq</th>
<th>ABSOLUTE Min P.W.</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D7215Z-xx</td>
<td>4.0 ± 1.0*</td>
<td>1.0 ± 0.5</td>
<td>27.8 MHz</td>
<td>18.0 ns</td>
<td>166.7 MHz</td>
<td>3.00 ns</td>
</tr>
<tr>
<td>3D7215M-xx</td>
<td>6.0 ± 1.0*</td>
<td>1.5 ± 0.7</td>
<td>23.8 MHz</td>
<td>21.0 ns</td>
<td>153.8 MHz</td>
<td>3.25 ns</td>
</tr>
<tr>
<td>-2</td>
<td>8.0 ± 1.0*</td>
<td>2.0 ± 0.8</td>
<td>20.8 MHz</td>
<td>24.0 ns</td>
<td>142.8 MHz</td>
<td>3.50 ns</td>
</tr>
<tr>
<td>-2.5</td>
<td>10.0 ± 1.0*</td>
<td>2.5 ± 1.0</td>
<td>18.5 MHz</td>
<td>27.0 ns</td>
<td>133.3 MHz</td>
<td>3.75 ns</td>
</tr>
<tr>
<td>-3</td>
<td>12.0 ± 1.0*</td>
<td>3.0 ± 1.3</td>
<td>16.7 MHz</td>
<td>30.0 ns</td>
<td>125.0 MHz</td>
<td>4.00 ns</td>
</tr>
<tr>
<td>-4</td>
<td>16.0 ± 1.0*</td>
<td>4.0 ± 1.3</td>
<td>13.9 MHz</td>
<td>36.0 ns</td>
<td>111.1 MHz</td>
<td>4.50 ns</td>
</tr>
<tr>
<td>-5</td>
<td>20.0 ± 1.0*</td>
<td>5.0 ± 1.4</td>
<td>11.9 MHz</td>
<td>42.0 ns</td>
<td>100.0 MHz</td>
<td>5.00 ns</td>
</tr>
<tr>
<td>-6</td>
<td>24.0 ± 1.0*</td>
<td>6.0 ± 1.4</td>
<td>10.4 MHz</td>
<td>48.0 ns</td>
<td>83.3 MHz</td>
<td>6.00 ns</td>
</tr>
<tr>
<td>-8</td>
<td>40.0 ± 1.0</td>
<td>8.0 ± 1.4</td>
<td>8.33 MHz</td>
<td>60.0 ns</td>
<td>62.5 MHz</td>
<td>8.00 ns</td>
</tr>
<tr>
<td>-10</td>
<td>50.0 ± 1.0</td>
<td>10.0 ± 1.5</td>
<td>6.67 MHz</td>
<td>75.0 ns</td>
<td>50.0 MHz</td>
<td>10.00 ns</td>
</tr>
<tr>
<td>-12</td>
<td>60.0 ± 1.2</td>
<td>12.0 ± 1.5</td>
<td>5.56 MHz</td>
<td>90.0 ns</td>
<td>41.7 MHz</td>
<td>12.00 ns</td>
</tr>
<tr>
<td>-15</td>
<td>75.0 ± 1.5</td>
<td>15.0 ± 1.5</td>
<td>4.42 MHz</td>
<td>113 ns</td>
<td>33.3 MHz</td>
<td>15.00 ns</td>
</tr>
<tr>
<td>-20</td>
<td>100 ± 2.0</td>
<td>20.0 ± 2.0</td>
<td>3.33 MHz</td>
<td>150 ns</td>
<td>25.0 MHz</td>
<td>20.00 ns</td>
</tr>
<tr>
<td>-25</td>
<td>125 ± 2.5</td>
<td>25.0 ± 2.5</td>
<td>2.66 MHz</td>
<td>188 ns</td>
<td>20.0 MHz</td>
<td>25.00 ns</td>
</tr>
<tr>
<td>-30</td>
<td>150 ± 3.0</td>
<td>30.0 ± 3.0</td>
<td>2.22 MHz</td>
<td>225 ns</td>
<td>16.7 MHz</td>
<td>30.00 ns</td>
</tr>
<tr>
<td>-40</td>
<td>200 ± 4.0</td>
<td>40.0 ± 4.0</td>
<td>1.67 MHz</td>
<td>300 ns</td>
<td>12.5 MHz</td>
<td>40.00 ns</td>
</tr>
<tr>
<td>-50</td>
<td>250 ± 5.0</td>
<td>50.0 ± 5.0</td>
<td>1.33 MHz</td>
<td>375 ns</td>
<td>10.0 MHz</td>
<td>50.00 ns</td>
</tr>
</tbody>
</table>

* Total delay referenced to Tap1 output; Input-to-Tap1 = 7.5ns ± 1.5ns

NOTE: Any dash number between 1 and 50 not shown is also available as standard product ©2002 Data Delay Devices
APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D7215 five-tap delay line architecture is shown in Figure 1. The delay line is composed of a number of delay cells connected in series. Each delay cell produces at its output a replica of the signal present at its input, shifted in time. The delay cells are matched and share the same compensation signals, which minimizes tap-to-tap delay deviations over temperature and supply voltage variations.

INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a Recommended Maximum and an Absolute Maximum operating input frequency and a Recommended Minimum and an Absolute Minimum operating pulse width have been specified.

OPERATING FREQUENCY

The Absolute Maximum Frequency specification, tabulated in Table 1, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The Recommended Maximum Frequency specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed. To guarantee the delay accuracy for input frequencies higher than the Recommended Maximum Frequency, the 3D7215 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.

OPERATING PULSE WIDTH

The Absolute Minimum Pulse Width (high or low) specification, tabulated in Table 1, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The Recommended Minimum Pulse Width (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in Table 1 is guaranteed.

To guarantee the delay accuracy for input pulse width smaller than the Recommended Minimum Pulse Width, the 3D7215 must be tested at the user operating frequency.
pulse width. Therefore, to facilitate production and device identification, the **part number will include a custom reference designator** identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

### POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D7215 delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The thermal coefficient is reduced to 200 PPM/C, which is equivalent to a variation, over the 0C-70C operating range, of ±1% from the room-temperature delay settings and/or 1.0ns, whichever is greater. The **power supply coefficient** is reduced, over the 4.75V-5.25V operating range, to ±0.5% of the delay settings at the nominal 5.0VDC power supply and/or 0.5ns, whichever is greater. **It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.**

---

### DEVICE SPECIFICATIONS

#### TABLE 2: ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Supply Voltage</td>
<td>V_{DD}</td>
<td>-0.3</td>
<td>7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Pin Voltage</td>
<td>V_{IN}</td>
<td>-0.3</td>
<td>V_{DD}+0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Pin Current</td>
<td>I_{IN}</td>
<td>-1.0</td>
<td>1.0</td>
<td>mA</td>
<td>25C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_{STRG}</td>
<td>-55</td>
<td>150</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>T_{LEAD}</td>
<td>300</td>
<td>C</td>
<td>10 sec</td>
<td></td>
</tr>
</tbody>
</table>

#### TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Supply Current*</td>
<td>I_{DD}</td>
<td>1.5</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Threshold Voltage</td>
<td>V_{TH}</td>
<td>2.2</td>
<td>2.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High Level Input Current</td>
<td>I_{IH}</td>
<td>1</td>
<td>\mu A</td>
<td>V_{IH} = V_{DD}</td>
<td></td>
</tr>
<tr>
<td>Low Level Input Current</td>
<td>I_{IL}</td>
<td>1</td>
<td>\mu A</td>
<td>V_{IL} = 0V</td>
<td></td>
</tr>
<tr>
<td>High Level Output Current</td>
<td>I_{OH}</td>
<td>-4.0</td>
<td>mA</td>
<td>V_{DD} = 5.0V</td>
<td>V_{OH} = 4.0V</td>
</tr>
<tr>
<td>Low Level Output Current</td>
<td>I_{OL}</td>
<td>4.0</td>
<td>mA</td>
<td>V_{DD} = 5.0V</td>
<td>V_{OL} = 0.4V</td>
</tr>
<tr>
<td>Output Rise &amp; Fall Time</td>
<td>T_{R} &amp; T_{F}</td>
<td>2</td>
<td>ns</td>
<td>C_{LD} = 5 pf</td>
<td></td>
</tr>
</tbody>
</table>

*_{I_{DD}}(Dynamic) = 5 \times C_{LD} \times V_{DD} \times F
  where: \ C_{LD} = Average capacitance load/tap (pf)
  F = Input frequency (GHz)
  Input Capacitance = 10 pf typical
  Output Load Capacitance (C_{LD}) = 25 pf max
SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 5.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 1.0V and 4.0V)
Pulse Width: PW_IN = 1.5 x Total Delay
Period: PER_IN = 3.0 x Total Delay

OUTPUT:
R_load: 10KΩ ± 10%
C_load: 5pf ± 10%
Threshold: 2.5V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

Figure 2: Test Setup

Figure 3: Timing Diagram